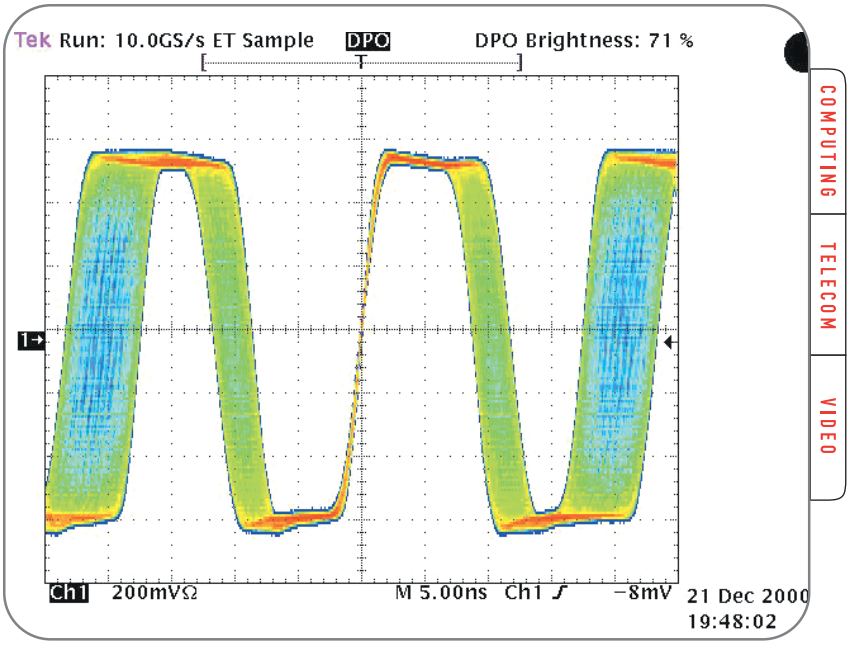
The Challenges Posed by Higher Clock Rates and Tighter Timing Margins



Introduction: Managing Jitter Ensures Robust Digital Designs

Digital designers are facing higher clock rates and tighter timing margins than ever before.

This trend creates extremely small design margins with little tolerance for clock or data jitter. New methods for characterizing and simulating jitter in digital designs are needed to keep pace with the increasing clock and data rates that are emerging. The Tektronix AWG500/600 Arbitrary Waveform Generators (AWG) and the DG2000 (DG) family of Digital Data Generators are a set of robust tools that help designers to simulate various types jittered signals. These products are used to uncover sources of unwanted jitter or permit the injection of controllable jitter into a circuit or system.

Jitter is a signal's variation from its ideal position in time or the timing variation from transition to transition that occur at a rate greater than 10 Hz. Excessive jitter can increase the bit error rate (BER) of a communications signal by incorrectly transmitting the data bit stream. Common sources of jitter are: the clock source, power supply noise, cross talk from adjacent traces, ground bounce, signal reflections, thermal noise, and improperly terminated transmission lines. Accurate measurement of jitter and injection of simulated jitter is necessary to determine how jitter tolerant a system is, or how close the circuit or system is to failing due to excessive jitter.

Tektronix AWGs and DGs are the instruments of choice for design and test engineers who are tasked with generating "real-world" signals that mimic the electrical signal environment the unit under test (UUT) could experience in actual use. An AWG is a sophisticated playback system that delivers waveforms based on stored digital data that replicate the changing voltage levels of an AC signal. AWGs combine a precise clock, an accurate digital to analog converter (DAC), and waveform memory that allow a wide range of signal shapes of varying frequency and amplitude to be created. Clocks generated by an AWG may be two level binary or sinusoidal in nature.

Tektronix Data Generators offer designers a set of tools for characterizing jitter and evaluating tight timing margins. DGs such as the DG2040 1.1 GHz Data Generator provide very low jitter clocks suitable for clock substitution, a useful jitter troubleshooting technique. DGs are similar to AWGs in that waveforms are contained in memory and are output with great precision. Unlike an AWG, a DG only generates two level binary signals. DGs contain sophisticated pattern sequencing that includes jumps, looping, and external event triggering that can be used to extend pattern memory or customize data flow to support virtually any application. Furthermore, the DG2040 has the ability to control all or selected edge timing in the data pattern, providing a very versatile data generator for applications requiring precise control of clock and data. An AWG or DG, when used in-conjunction with Tektronix TDSJIT1 or TDSJIT2 Jitter Analysis Software on the TDS7000/600/700 series oscilloscopes, provides a jitter generator/analysis system to apply to troubleshooting of design faults that may be jitter related.

(1) www.tektronix.com/signal_sources/

Tektronix

AWGs: Simplify the process, find a solution

Tektronix's AWGs come equipped with a number of utilities that simplify the process of creating clock signals with precise jitter. Determining which method to use depends on the type of signal and jitter designers need to generate. These utilities fall into several categories:

- Clock Substitution
- Equation Script Editing
- Jitter Composer Application
- Waveform Sequencing

Clock Substitution

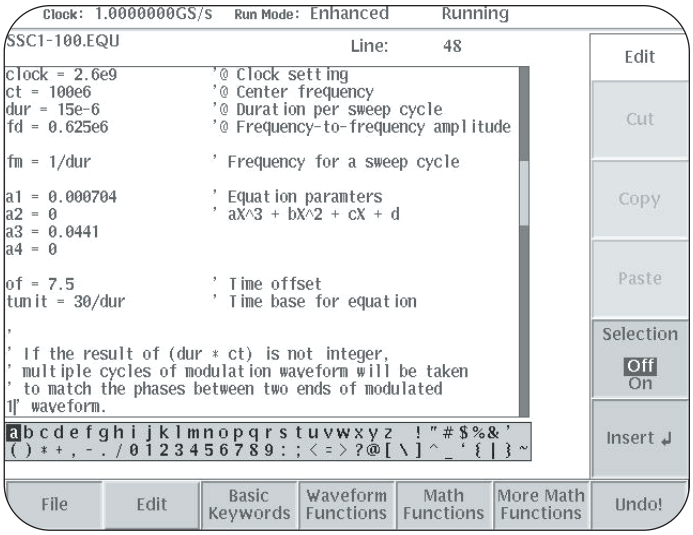
For applications where designers want to eliminate various possible sources of jitter within a system, an external clock with ultra low jitter permits substitution for the internal clock. For this purpose, a clock is defined as a periodic, two level AC signal of fixed frequency. The inherent jitter of an AWG generated clock signal is primarily a function of the AWG's sample clock stability. The sample clock contributes most to the base line jitter specification of an AWG.

The Tektronix AWG610 2.6 Gs/s AWG can generate simple clocks with jitter as low as < 6 ps RMS. Assuming the jitter in the system is now reduced because of the substitute clock generated by the AWG, faults in the internal clock circuit could be the cause. If the jitter is not reduced, the internal clock circuit is not the cause of jitter, and further investigation is required into other causes.

Equation Script Editing

Designers are using jittered or modulated clocks to reduce EMI in personal computers and other devices subject to strict EMI regulations. This type of clock is commonly termed a Spread Spectrum Clock (SSC). Equation Script Editing in Tektronix AWGs provide an easy method for designers to create the complex waveforms needed to simulate SSC as they seek to reduce EMI levels in their designs.

Equation editing permits designers to create waveforms based on a polynomial equation entered into the AWG. Using the equation script editor, complex modulated waveforms such as a SSC can be created.



▶ ***Figure 1.*** *The Equation Script Editor calculates waveforms based on user defined polynomial equations.*

When a polynomial equation is entered into the editor, it compiles the equation, calculates, and stores the resulting data points in memory. The waveform can be saved onto the AWG's hard drive. A variety of spread spectrum waveform examples are included with the AWG and are also available from the Tektronix Technical Support Center:

Function 1:	"Hershey Kiss" profile
Function 2:	Square function profile
Function 3:	Triangle function profile
Function 4:	Sin function profile
Function 5:	Sin + a*Sin(b) function profile
Function 6:	Gaussian pulse function profile

The signal frequency ranges from 10 MHz to 100 MHz. Equation files are ASCII based and can be modified to meet the designer's specific needs. The filename of each .equ file describes the resulting waveform frequency and modulation profile. The file ssc2-100.equ for example, creates waveforms that produce a signal with a square function at 100 MHz.

Each equation file generates following waveform files:

SSCx-yyyB.wfm: Modulation function

SSCx-yyyF.wfm: Integration of modulation function (may be multi-cycles)

SSCx-yyyC.wfm: Carrier signal

SSCx-yyyS.wfm: Modulated signal.

SSC equation files generate a sine waveform as the carrier signal. Using a sine waveform as the carrier greatly simplifies the calculation and generation of the modulated signal. In most cases, a sinusoidal waveform correctly offset can be used in place of a square wave as the clock signal.

The various parameters used in the SSC Equation files are:

Clock: Clock frequency to be set in the AWG

ct: Center frequency. This is the same as the carrier frequency.

Important: The ratio (clock/ct) will be equal to or larger than 8.

dur: Duration for modulation (sweep) cycle.

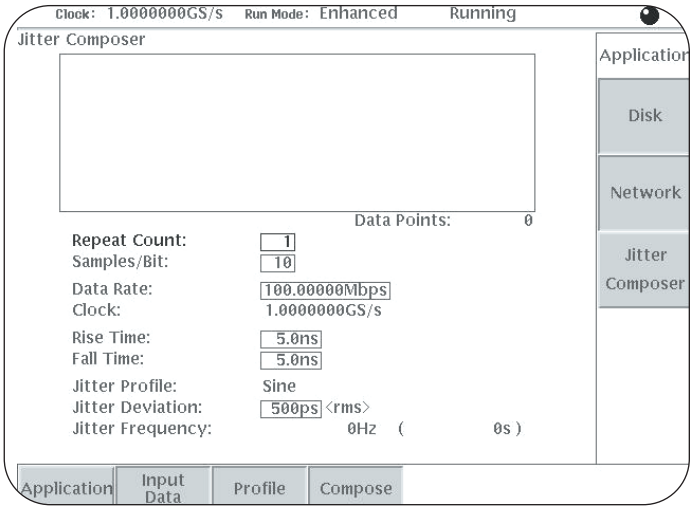
Important: The result of (ct*dur) must be an integer or its decimal place must be 0.5, 0.25, 0.125 or 0.1 to match the phases between two ends (start and end) of modulated waveform to be generated. fd: Frequency deviation from center frequency

The parameters above are common to all SSC equations. These parameters can be changed to fit individual requirements.

To generate Spread Spectrum Clock signal, complete the following steps:

1. Select an equation file according to the type of modulation function needed.
2. Modify the equation parameters using the Equation Script editor as necessary.
3. Save the file to the AWG's internal hard drive.
4. Compile the file.
5. Load the resulting waveform file from the AWG's hard drive. Look for a file with this file name format "SSCx-yyyS.wfm". Note the S in the filename signifies that this waveform is the fully modulated carrier waveform.
6. Start output.

Jitter Composer Application



▶ ***Figure 2.*** *Jitter Composer menu uses a simple fill-in-the-blanks interface.*

To create a jittered clock or two-level binary signal, use the Jitter Composer application built into the AWG500 series or the AWG610. This application creates signals with jitter and SSC relative to a 0 and 1 bit-pattern. Jitter Composer differs from the Equation Script Editor because the Jitter Composer is limited to two-level binary waveforms, whereas the Equation Script Editor allows users to create equations that generate any waveform that can be mathematically described.

Signals are created using the following process:

- Input binary bit pattern expressed by 0 and 1.
- Data is created for one period by sorting the bit pattern in the direction of the time base per user set parameters.
- Deviate the data for one period in the direction of time base along the selected Jitter Profile.

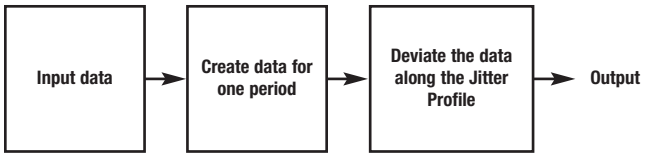
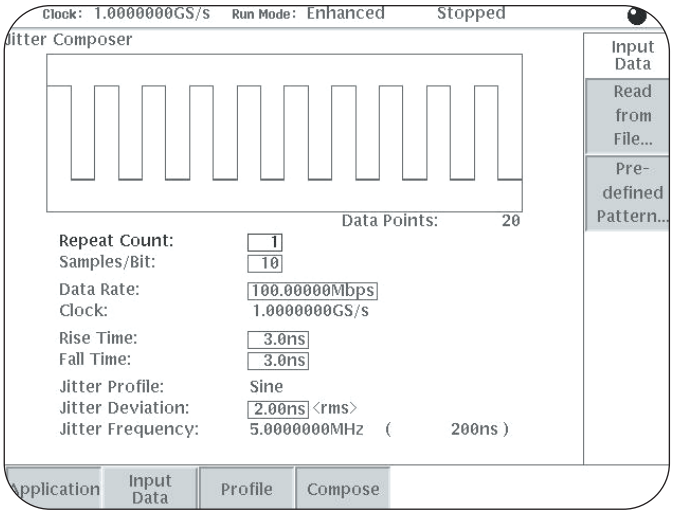


Table 1 describes the various user defined parameters in the Jitter Composer Application.

Parameters	Descriptions
Repeat Count	Specifies the repetition number of original waveform points that makes up one period for jitter waveform.
Samples/Bit	Specifies the number of points to be generated for each point of the input data. The value is larger than 2 because the input data needs rise time and fall time.
Data Rate [bps]	Specifies the data rate for jitter waveform. This value is prior to Samples/Bit, Rise Time, and Fall Time.
Clock [Samples/s]	Display clock rate (display only). The clock rate is automatically set by Data Rate x Samples/Bit.
Rise Time	Specifies rise time of pulse (time between points of 10% and 90% level of amplitude). You can select 0(zero). One restriction is applied to Rise Time parameter; Rise Time + Fall Time ≤ 1/Data Rate x 2 x 4/5.
Fall Time	Specifies fall time of pulse (time between points of 10% and 90% level of amplitude). You can select 0(zero). One restriction is applied to Fall Time parameter; Rise Time + Fall Time ≤ 1/Data Rate x 2 x 4/5.
Jitter Profile	Specifics the deviation of each point for one period in the direction of time base. Use Profile (bottom) → Sine, Triangle (side) menu to select among sine wave and triangle wave.
Jitter Deviation	Specifies the deviation of jitter waveform. Suppose 10101010....repetitive pattern as an input data, and one 1,0 pair as one period of pattern, this value represents the equivalent deviation for one 1,0 pair.[1]
Jitter Frequency	Display repeated frequency of jitter waveform. This value is automatically set by Clock / Total Points.
Data Points	Display the number of points for input data (display only).
Total Points	Display the number of points for jitter waveform (display only). This value is automatically set by Data Points x Repeat Counts x Samples/Bit.

[1] Jitter deviation on peak-to-peak is:
profile = sine: about 2.83 times of jitter deviation on rms.
profile = triangle: about 3.45 time of jitter deviation on rms.



▶ ***Figure 3.*** *Input Data Screen.*

Figure 3 shows the data input menu. Binary data can be user defined or selected internally from a variety of formats ranging from pseudo-random bit sequences to fixed alternating 1s and 0s.

Table 2 Available Data Patterns

Pattern items	Descriptions
PN9	9-bits M-series pseudo random pulse.
PN15	15-bits M-series pseudo random pulse.
100100	
10001000	
1000010000	
1010101010	
100000100000	
1000000010000000	

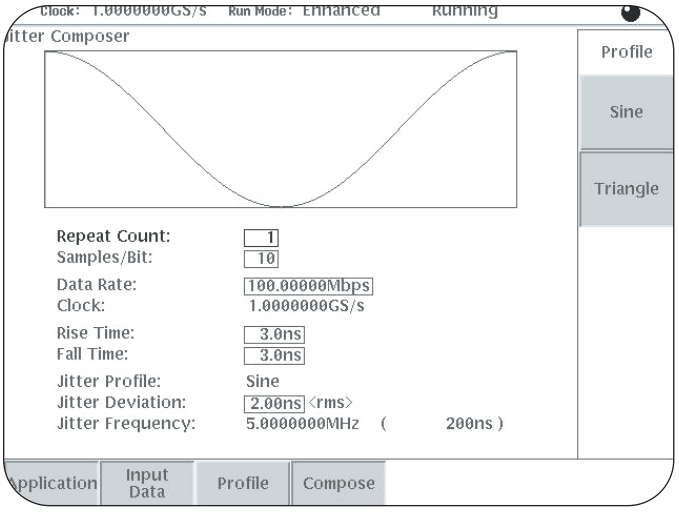


Figure 4. *Jitter Profile Input screen*

A sine or triangle jitter profile can be selected. The jitter profile describes the distribution of jitter across the signal of interest.

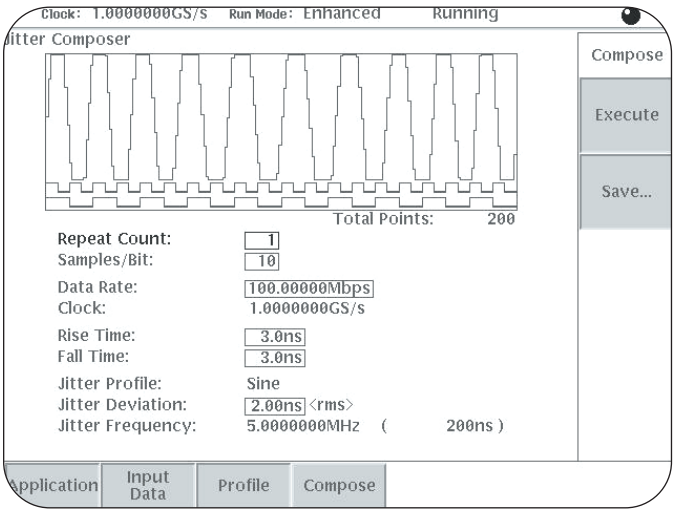


Figure 5. *Final menu screen used to compile and save the waveform.*

The Compose menu shown above compiles the jitter waveform and is saved as a .wfm waveform file on the AWG's hard drive.

A jittered 50 MHz clock (or 100 Mbps data stream) modulated using a triangle profile created with the Jitter Composer application is shown below.

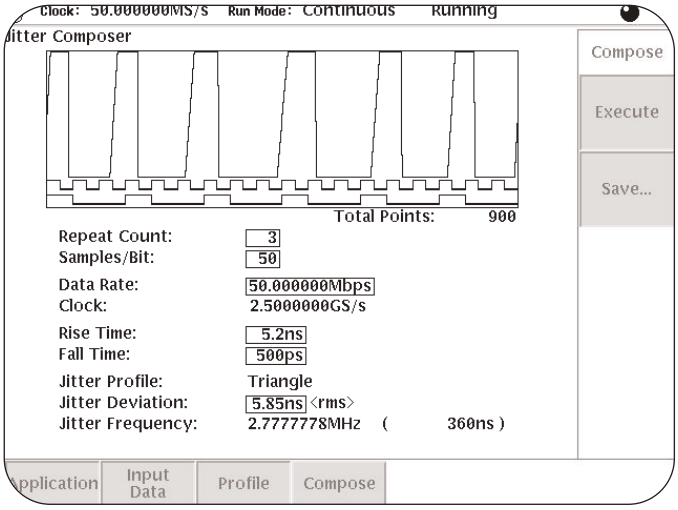


Figure 6. *Jittered 50MHz clock screen.*

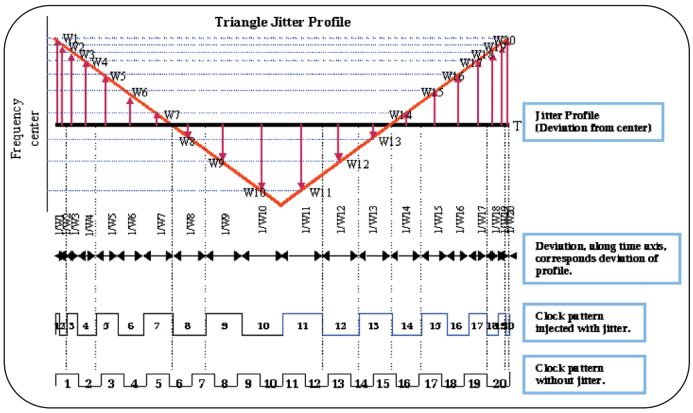


Figure 7. *Frequency domain display of a jittered clock.*

The diagram above illustrates how each bit time is incrementally lengthened or shortened according to the modulation profile.

The following data or conditions were set to create this waveform.

1. A 20 bit binary pattern is defined as alternating 1s and 0s:
   "10101010101010101010"
2. The number of samples per bit is set to 10. This means that for every 1 or 0 in the pattern, a total of 10 AWG samples are stored in memory. The amount of waveform memory consumed by this pattern will be 200 memory locations. (20 bits * 10 samples per bit = 200 samples)

3. Based on the entry of 100 Mbps and 10 samples per bit, the application automatically calculates the sample clock rate of 1 GS/s. (100 Mbps * 10 samples per bit = 1000 Ms/s).
4. Recognizing that the 20-bit pattern establishes one period of the modulation frequency, the modulation frequency can be calculated (1000 MS/s / 200 samples = 5 MHz frequency of modulation). Increasing the number of samples per bit has the effect of decreasing the modulation frequency.
5. Rise and fall times are set independently based on user input. Sufficient samples per bit are needed to accurately set the transition times.

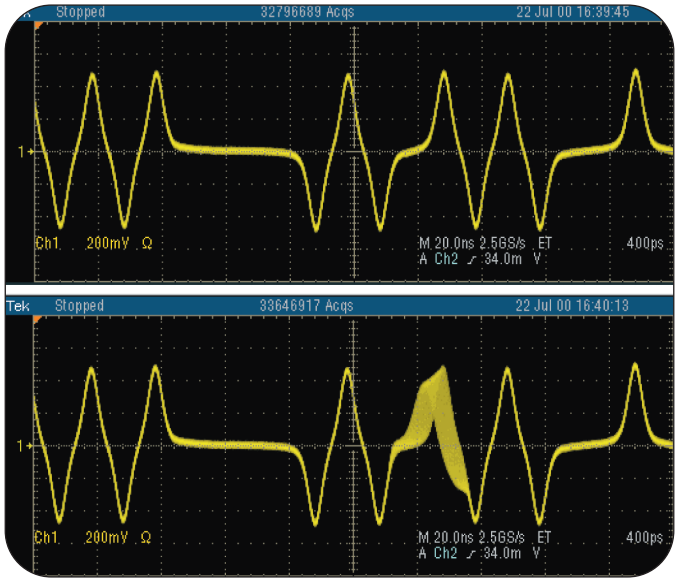
After execution of the Jitter Composer, each bit time value of W1 through W20 will be lengthen or shortened as dictated by the jitter modulation applied.

Example of Effects of Jitter on Individual Bit Times:

At bit location W1, the jitter deviation delta is calculated to be –1.2 ns. This value is summed with the nominal value of 10 ns (period of bit time at 100 Mbps) resulting in a bit time of 8.8 ns. At location W2, the delta value is –0.8 ns that again are summed with the nominal value of 10 ns resulting in a bit time of 9.2 ns. Thus the period of W1 and W2 is 8.8 ns + 9.2 ns = 55.6 MHz. This results in a delta of 5.6 MHz from the nominal frequency value of 50 MHz. This is the maximum positive excursion in bit timing. As the influence of the modulation profile approaches W7, the delta time becomes zero. As the modulation profile advances to W11, the delta time reaches maximum negative excursion in bit timing as shown in the following calculations. At bit location W11, the jitter deviation delta is calculated to be 1.9 ns. This value is summed with the nominal value of 10 ns resulting in a bit time of 11.9 ns. At location W12, the delta value is 1.6 ns that is again summed with the nominal value of 10 ns resulting in a bit time of 11.6 ns. Thus the period of W11 and W12 is 11.9 ns + 11.6 ns = 42.6 MHz. The resulting delta of 7.4 MHz from the nominal frequency value of 50 MHz is the maximum negative excursion in bit timing.

Waveform Sequencing

Powerful editing features and Waveform Sequencing of the AWG allow the designer to selectively apply jitter to portions of a waveform. This technique permits evaluation of jitter in disk drive read channel applications.

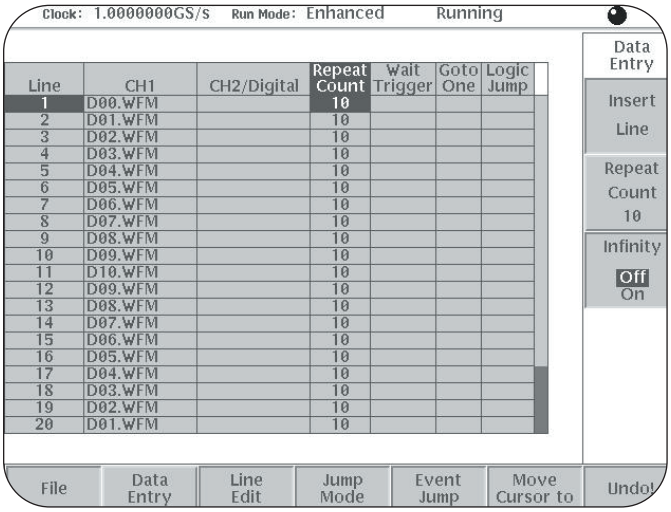


▶ ***Figure 8.*** *The top waveform is the original. The bottom waveform shows how jitter can be applied to specific bits of a simulated disk drive data stream.*

The technique used to inject jitter into a specific portion of the waveform uses two built-in functions of the AWG500 series and AWG610. These functions are the Quick Editor and waveform sequencing.

The Quick Editor lets you modify and/or output any part of a waveform you are currently editing with the Waveform Editor. The data between cursors can be scaled or shifted vertically and/or horizontally (Expand/Shift). To apply the Quick Editor to a portion of the waveform, set the waveform cursors to delineate the portion of the waveform you wish to modify. Using the AWG's front panel horizontal and vertical controls, you can easily modify the timing in the horizontal axis and the amplitude in the vertical axis. Save the modified waveform and repeat as necessary to build up a library of time and amplitude shifted waveforms.

The next step involves use of the waveform sequencing function. Waveform sequencing describes the ability of the AWG to output a specific list of waveform files in order and in real-time without latency. When using waveform sequencing, it is important to align the amplitude of sequential waveforms so as to not to introduce discontinuity at the waveform boundaries.



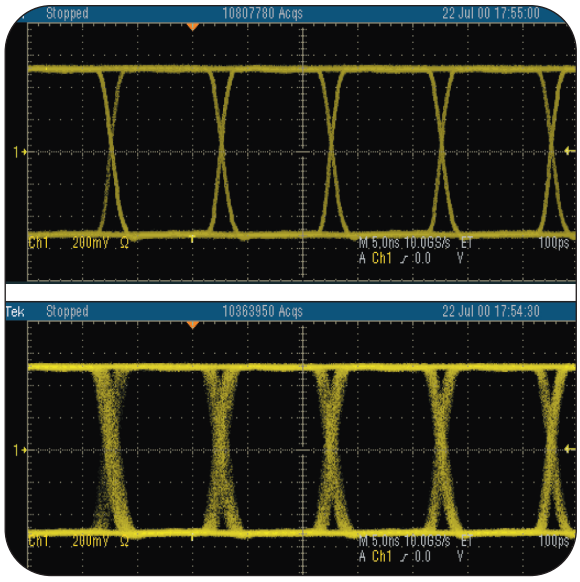
Line	CH1	CH2/Digital	Repeat Count	Wait Trigger	Goto One	Logic Jump
1	D00.WFM		10			
2	D01.WFM		10			
3	D02.WFM		10			
4	D03.WFM		10			
5	D04.WFM		10			
6	D05.WFM		10			
7	D06.WFM		10			
8	D07.WFM		10			
9	D08.WFM		10			
10	D09.WFM		10			
11	D10.WFM		10			
12	D09.WFM		10			
13	D08.WFM		10			
14	D07.WFM		10			
15	D06.WFM		10			
16	D05.WFM		10			
17	D04.WFM		10			
18	D03.WFM		10			
19	D02.WFM		10			
20	D01.WFM		10			

▶ ***Figure 9.*** *This figure illustrates a waveform sequence list. Each waveform output is repeated 10 times before the next waveform in the sequence is output.*

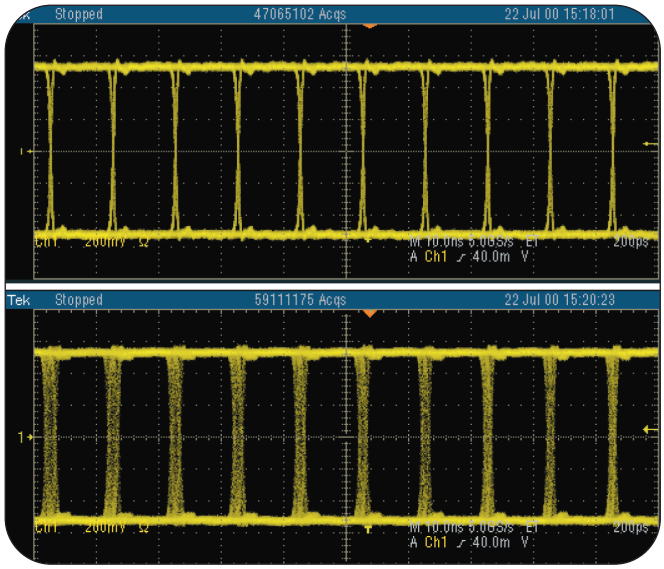
Waveform sequencing and the Quick Editor provide the designer a fast and efficient method to insert apparently random aberrations into the waveform stream.

Using an external clock or time base reference to create jitter

Wander and Phase Jitter can be injected into the AWG waveform through the use of either an external clock or the 10 MHz time base reference input of an AWG. The external clock input of the AWG is used as a substitute for the internal sample clock. If the external clock is a modulated source, such as the output from a FM modulated RF signal generator, and then the timing of waveform samples output by the AWG will vary directly proportionally to the external clock frequency and phase. Similarly, if the AWG has a 10 MHz reference clock input, an externally modulated 10 MHz reference will cause a similar effect. However, the 10 MHz reference input has a much narrower range of modulation due to the phase locking range of the PLL used in the internal sample clock generator.



▶ ***Figure 10.*** *The top oscilloscope trace shows a data stream simulated by the AWG. The bottom trace shows the same data stream with jitter applied through the use of a modulated 10 MHz reference.*



▶ ***Figure 11.*** *The top trace shows the AWG waveform using the internal sample rate clock. The bottom trace is jittered by substituting an external sample rate clock that is FM modulated.*

The DG2040 1.1GHz Data Generator: create jitter with edge control

The DG2040 1.1GHz Data Generator offers designers a whole new set of tools for characterizing jitter, setup, and hold timing margins. Sophisticated pattern sequencing that includes jumps, looping and external event triggering can be used to extend the deep memory or customize data flow to support virtually any application. Used in conjunction with Tektronix jitter analysis software (TDSJIT1 and TDSJIT2) for the TDS7000, TDS700, and TDS600 oscilloscopes, the designer now has a fully functional jitter generator/analysis system. Furthermore, the DG2040 has the ability to control all or selected edge timing with Sony/Tektronix exclusive Edge Control function. The DG2040 is a very versatile data generator for applications requiring the precise timing control of clock or serial data signals.

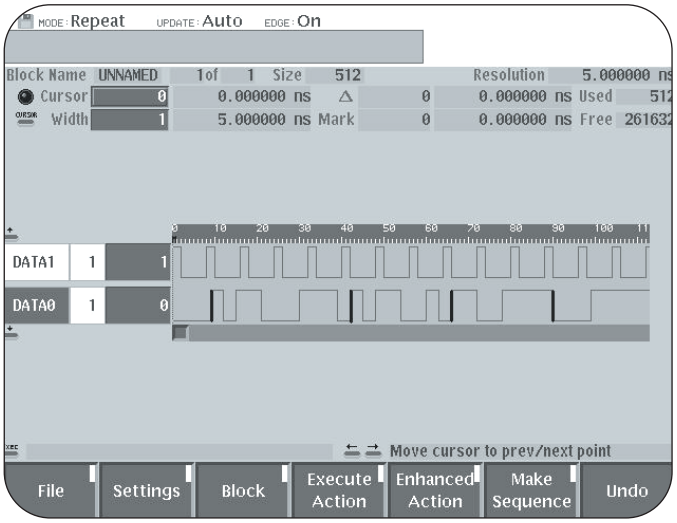
Data transitions where you want them

The DG2040's Edge Control function offers the ability to retard by ± 100 ps in 5 ps steps or continuously jitter the relative timing of selected edges of the data stream. This feature is particularly useful when evaluating setup and hold timing margins, injecting clock jitter into a digital circuit, or evaluating conditions of metastability.

▶ ***Figure 12.*** *A portion of the Edge Control Menu allowing static control of identifies edge position +/- 100 ps in 5 ps steps.*

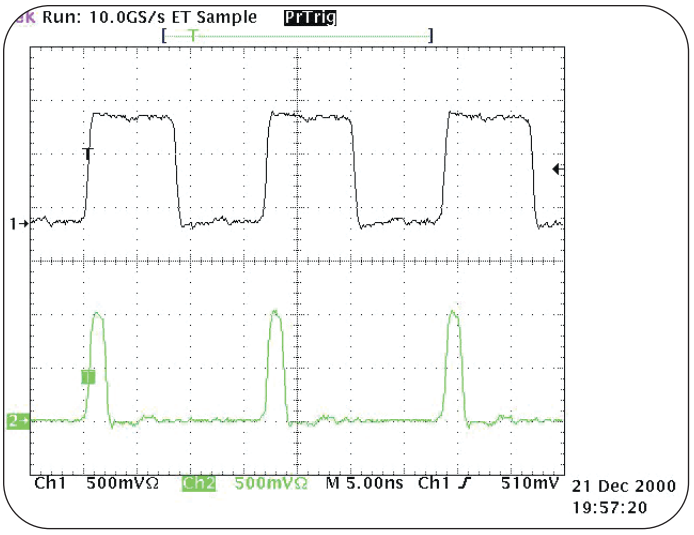
Unique timing control

The DG2040 offers two methods to change edge timing through the Edge Control Function: static edge control and continuous edge control. In both modes, one channel of the DG2040 determines the edge(s) affected by the edge control function on the second channel. This permits the design engineer to create a serial data stream or clock signal with finely controlled edge placement useful in metastability or clock/data jitter margin characterization. Figure 12 shows the edge control menu, illustrating how the user may specify a static edge position of the data pattern by entering a time or position offset.

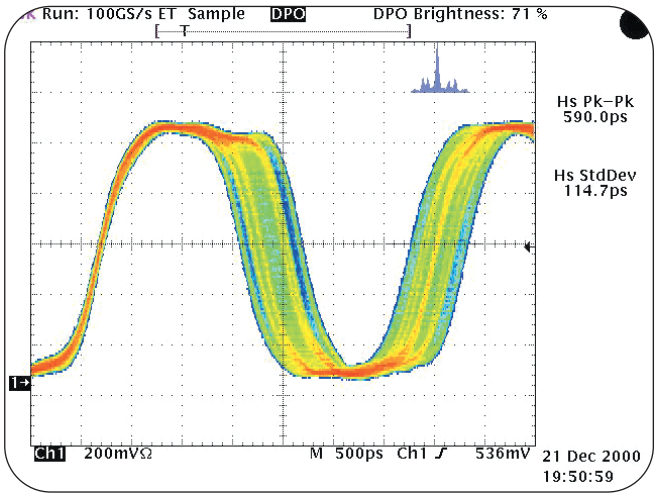


▶ ***Figure 13.*** *Illustrates how the user identifies specific edges of the DATA0 data pattern by using DATA1 as an edge-identifying template.*

The Edge Control function also permits an external modulating signal to continuously jitter selected edges by up to ± 100 ps. This is useful in evaluating the effects of jitter on your digital design.



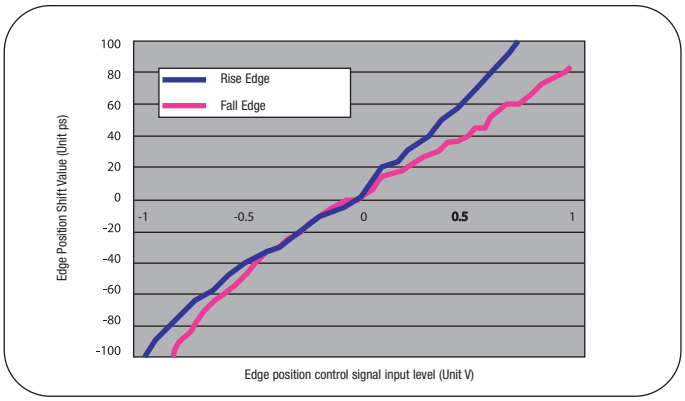
▶ ***Figure 14.*** *Oscilloscope screen shot of the DG2040 DATA1 control bit alignment.*



▶ ***Figure 15.*** *The effect of adding continuous modulation (jitter) to both rising and falling edges of a pulse.*

Different jitter profiles

The external modulation signal's amplitude controls the amount of time shift applied to the selected edges shown in figures 14 and 15. The engineer may find a jitter distribution other than sinusoidal to be desirable. If an AFG310 or AWG510 is used, a modulation profile other than a sinewave is possible. The frequency of the modulation signal may range from DC to 500 MHz.



▶ ***Figure 16.*** *This chart represents the transfer function between amplitude and the magnitude of the time shift.*

Table 3 DG2040 Time Position Offset Setup

1. Enter a master clock rate for the DG2040.
2. Create a clock pattern, 10 bits high and 10 bits low for DATA0.
3. Create a data pattern for DATA1 such that logic 1 is set at a bit position corresponding to a rising (or falling) edge on DATA0. See figure 13.
4. Enable Edge Control ON from the Application Menu.
5. Enter a time shift into the Position Offset menu item. See figure 12.

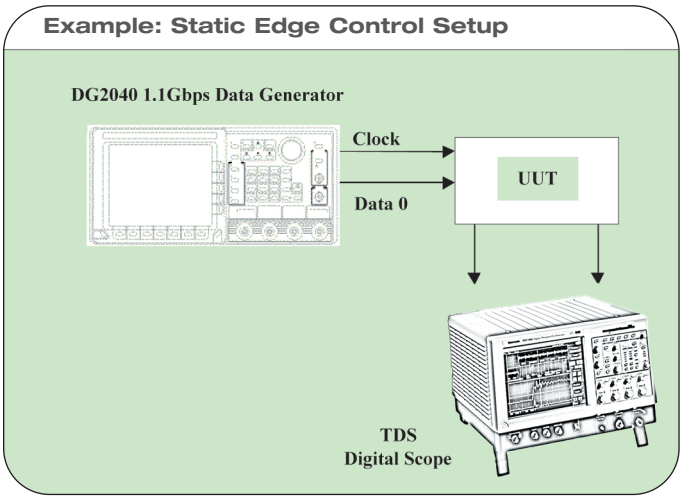


Figure 17. *Equipment setup*

Figure 17 shows a typical setup to inject a precise time position offset between the DG2040 CLOCK out and the DATA0 out. Table 3 outlines the steps needed to program the DG2040 for this application

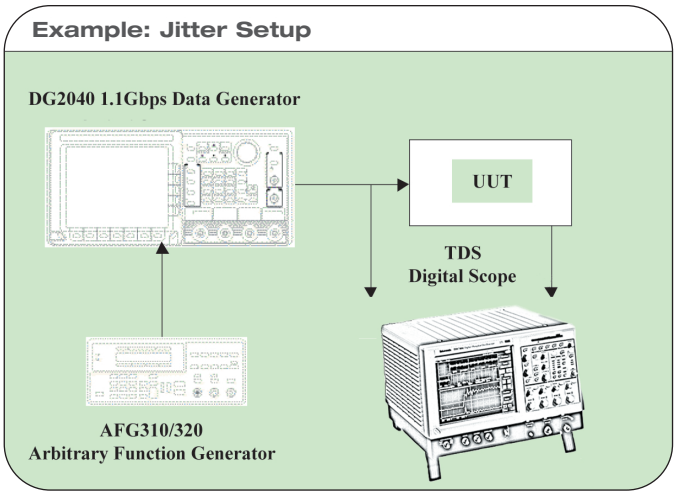


Figure 18. *A typical jitter test setup.*

The DG2040 is setup as shown in figure 18. Table 4 outlines the DG2040 front panel menu setup. An AFG310 provides the modulation signal to the front panel Edge Control BNC input of the DG2040. Configure the AFG310 to provide a suitable jitter profile (sine, ramp, or Gaussian).

Table 4 DG2040 Jitter Setup

1. Create a clock pattern for channel 0 with a 50% duty cycle (101010…).
2. Create a clock pattern for channel 1 with a 25% duty cycle (100010001…).
3. Shift channel 's data one bit to the left with the shift data left function.
4. The pulse in channel 1 now lines up and over the rising edge of each data bit in the channel 0's clock pattern.
5. Set the arbitrary function generator to output a ± 1v sinewave signal at the switching frequency of the power supply and connect it to the Edge Control front panel BNC.
6. Press the Application front panel button to bring up the Edge Control menu. From the Edge Control menu select Edge Control ON.
7. With the TDS784D in DPO mode, note the jitter now apparent on the rising edge of the clock output on channel 0.

Simulate switching power supply caused jitter

Unacceptable jitter can result when unwanted noise at the switching frequency of a power supply couples to a digital system's clock or data lines. To evaluate a design's susceptibility to this kind of jitter, simulate switching power supply induced jitter with the DG2040 and a function generator.

Figure 18 illustrates the connection of equipment to simulate jitter on a clock of serial data stream. Channel 1 of a TDS7404 DPO Oscilloscope is shown connected to the DG2040 DATA0 output while channel 2 of the scope is connected to the UUT output. Use the TDSJIT2 Jitter Analysis option for the TDS7404 to analyze the time shift or jitter and the effects on the UUT.

For further details on specifications and setup of the various functions described in this application note please refer to the DG2040 User Manual, Tutorial section.

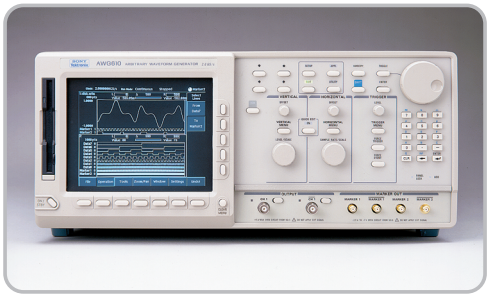
Product brief of the DG2040

The DG2040 1.1GHz Data Generator offers designers two complementary data outputs plus a complementary clock output. Output levels are variable from –1.25 V to +3.5 V with a maximum of 2.5 Vp-p. Deep memory of 256K bits per channel allow long, complex data patterns to be output. Sophisticated pattern sequencing that includes jumps, looping, and external event triggering can be used to extend the deep memory or customize data flow to support virtually any application. Data may be entered or edited directly from the large CRT screen either in parallel or serial format. The DG2040 offers very flexible timing control ranging from programmable delay of –1 ns to +2 ns with 10 ps resolution. Period jitter (clock out) is specified to be < 3.0 ps rms (typical). In addition, the ability to control all or selected timing of edges proves the DG2040 to be a very versatile data generator for applications requiring precise timing control of clock or serial data signals.

Conclusion

The AWG is a powerful ally in the battle to detect and eliminate jitter in communication systems and digital circuit designs. Using AWGs to provide ultra low jitter clocks can eliminate potential sources of jitter and help point out other areas to concentrate the investigation. AWGs are an excellent source to simulate Spread Spectrum Clocking. SSC clocks can reduce peak-radiated emissions helping to meet stringent EMI regulations while reducing the need for costly shielding. Possible sources of unwanted jitter were discussed and suggestions on how jitter can be reduced by paying attention to trace routing, shielding, and reducing reflections in high frequency transmission lines. This application note describes a number of methods where arbitrary waveform generators can be used to simulate precise jitter profiles for communications, digital design, clock simulation, and disk drive design.

The data generator while similar in function to the AWG, provides a 2 level binary signal that the user may jitter. The Edge Control function is an easy to use method to evaluate susceptibility to jitter caused by switching power supplies. Edge Control is also used to evaluate setup and hold conditions of digital components. Additionally, the ultra low jitter clock produced by the DG2040 can be used in clock substitution applications to eliminate the internal clock as a source of jitter.



▶ ***AWG610***

▶ ***DG2040***

▶ ***TDS7000***

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